Voltage-Lift Technique Based Non-Isolated Boost DC-DC Converter: Analysis and Design

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***Abstract*—In this paper, a new structure of non-isolated boost dc-dc converters based on voltage-lift (VL) technique is proposed. In comparison with conventional non-isolated boost dc-dc converters, the proposed converter generates higher voltage gain. In this paper, the relations between voltage and current of all elements in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are calculated as well as voltage gain in each mode. Then, the critical inductance and stress of switch current are extracted. Finally, the validity of given theories is examined by using the experimental results.**

***Index Terms*—Dc-dc converter, non-isolated boost converter, critical inductance, voltage-lift technique.**

I. Introduction

NOWADAYS, using dc-dc converters are rapidly expanding in computer systems, medical equipment, servo-motors, LED lighting systems, power factor correction (PFC), communication systems, hybrid vehicles auxiliary equipment, portable electrical equipment such as mobile phones and portable computers, uninterrupted power supplies (UPS) and green energy systems such as systems fuel cell, photovoltaic (PV) systems and wind turbine (WT) systems [1]. These types of power electronic converters are controlled using pulse width modulation (PWM) and switching frequency. The converters that switching is controlled by PWM technique are classified into two isolated and non-isolated groups. In the structure of isolated dc-dc converters such as fly back, forward, half bridge, full bridge and push pull, high-frequency transformer is used and achieving high voltage is possible by changing the number of turns of transformer. However, high-frequency transformers in addition to raising the prices leads to high switching voltage and considerable losses due to transformer leakage inductance [2]. To reduce this problem, non-dissipative snubber circuits or active clamp circuits are used that increases the price and size of the converters and complicates the control process [3]. In the structure of non-isolated dc-dc converters such as buck, boost, buck-boost, CUK, and SEPIC converters, there is no high-frequency transformer and as a result, non-isolated dc-dc converters have lower price, smaller size and lower switching losses and high efficiency [1].

Among non-isolated dc-dc converters, the conventional non-isolated boost converter due to high voltage gain, direct connection of inductor at input, and lower input capacitance at output and smaller filter size, switch protection against overvoltage and electromagnetic interference (EMI), lower power stress on the elements, higher transient response ratio, higher efficiency and power density has many applications in LED lighting systems, [4], PFC [5], auxiliary equipment of hybrid cars [6] and green energy systems [7] such as fuel cell systems, PV systems and WT systems. In these applications, the non-isolated boost converter acts as an interface between low-voltage sources and high-voltage load and plays an important role in increasing the output voltage gain from low voltage. Assuming that the converter is ideal in theory, and is in CCM, very high voltage gain would be achieved of a conventional non-isolated boost converter for high duty cycle ratio. However, due to substantial switching and conduction losses of the diodes and decrease in efficiency with increase of the voltage gain, especially in high loads, restoring the problem in the high voltage EMI of elements and high voltage stress of switching, rate of duty cycle is about 0.8 and voltage gain is almost limited to four times [8]. Therefore, the use of conventional non-isolated boost converters in high voltages would not be appropriate. To overcome these problems and improve the profile of these converters many methods and techniques have been presented in recent years.

In [9-10], new structures have been presented for non-isolated dc-dc boost converters. Although using this technique voltage gain is increased properly but in the higher voltage gains, the number of elements and voltage stress of switches is increased and its control system design becomes more complex. This technique has been developed in [11] to reduce voltage stress of switches. In [12-13], coupled inductor has been used to increase the voltage gain. This method can achieve high voltage gain and high efficiency by changing the coupled inductor turns ratio and energy recovery of leakage inductance. In addition, low off-state voltage can be provided by this method for the main switch [13]. Most of these converters have a high input current ripple and need a large input filter. As a result, the application of this method is limited. In addition, the diode reverse recovery time delay due

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to leakage inductance of coupled inductor; increase in size and price are other drawbacks of this method [14].

The non-isolated dc-dc converters that are connected in series and parallel have been presented in [15-16]. The purpose of this method is to achieve high voltage and high efficiency with wide rate of changes using the minimum number of active switches. This technique is used for applications in renewable energy. High losses, current ripple over the switches, and high stress of current and voltage of switches a well as semiconductor elements, lack of adequate performance at low voltage, complex control of switching, large size and high price and stability are the drawbacks of this technique. To reduce high stress of switches and semiconductor elements, coupled inductor is used in [17].

In the switched capacitor (SC) technique [18], the high-voltage gain is provided by the combination of a number switches and capacitors with minimum inductors. This technique has been developed in [19]. Although using this technique provides high voltage gain with high efficiency, with an increase in the rate of voltage gain switching control would be complicated due to the increased number of switches and capacitor, and current ripple is increased considerably. In addition, switching losses due to hard switching of active switches is disadvantage of this technique. In [20], a structure is provided using combination of a number of capacitors and diode to reduce switching complexity control and ripple current. In [21], switches and elements stresses have significantly decreased by using a coupled inductor.

In [22], high-frequency transformer or coupled inductor interleaving technique has been presented. In this technique, high-frequency transformer or coupled inductor is inserted between dc-dc converters such as boost-flyback, flyback-SEPIC, etc. to increase voltage gain [23]. This technique is applicable in most techniques of voltage boost such as VL and SC techniques [24]. This structure with changing the rate of inductor and recovery of the stored energy in leakage inductance of the high voltage gain provides high efficiency and low off-state voltage for switches. In most of these structures, passive and active clamp circuits are used to recover leakage inductance and to clamp voltage the off-state voltage of switch [25]. In the structure presented in [26], it is tried to eliminate the input current ripple by a transformer.

In [27], VL technique has been introduced. This technique has been extended in [28-29] as well. VL technique is a popular and effective technique for increasing the output voltage gain that has been used extensively in the power electronics circuits. Using this technique, characteristics of conventional non-isolated boost dc-dc converters are well improved. Using this method, the input voltage increases step to step to transfer high voltage gain to load. The performance of VL technique is based on energy storage elements (inductor and capacitor). High power density, high efficiency, simple structure and cheapness compared to other techniques and small output voltage ripple, especially for high voltage values are the features of this technique. In addition, the lack of additional switches that lead to the complexity of the control system of a dc-dc converter is an important feature of this technique.

In this paper, a new structure for non-isolated boost dc-dc converter based on VL technique is proposed that has higher voltage gain. In the followings, equations for elements of the proposed non-isolated boost dc-dc converter in CCM and DCM are extracted, and the voltage gain and critical inductance between CCM and DCM for proposed dc-dc converters are calculated. Then, the current stress of switch in CCM and DCM is evaluated. Finally, the accuracy of theoretical concepts will be evaluated by experimental results of a laboratory prototype.

II. The Proposed Structure

The structure of proposed converter is shown in Fig. 1. According to Fig. 1, the structure of the proposed converter consists of one power switch, two inductors, three capacitors and three diodes. For the convenience of analysis, the following assumptions are made: (a) The proposed converter is analyzed in the steady state, (b) The output voltage is constant, (c) The capacitors are large enough, so, the voltage of capacitors is assumed to be constant in each switching cycle, d) The switch and diodes are ideal. The voltage and current relations of each element in CCM and DCM are determined in the following.

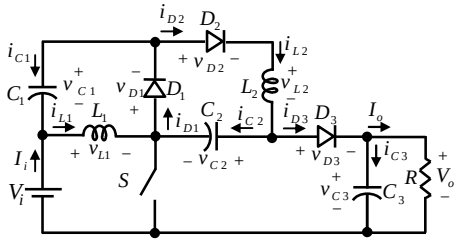

Fig. 1. Proposed converter

A. Operating Principle

Equivalent circuits and the key waveforms of the proposed converter under CCM and DCM are shown in Figs. 2, 3 and 5, respectively. The CCM consists of three operating mode including T_{on}, the first part of time interval of T_{off} (T'_{off}) and the second part of time interval of T_{off} (T''_{off}). While the DCM is made up of four operating mode including $(t_0,\ t_1)$, $(t_1,\ t_2)$, $(t_2,\ t_3)$ and $(t_3,\ t_4)$. The operating principle of proposed converter in CCM and DCM is discussed in the following.

Mode I: In the time interval of T_{on} in CCM and $(t_0,\ t_1)$ in DCM when the switch S is turned on and the diodes of D_1 and D_3 are reverse-biased and the D_2 diode is forward-biased, the inductor L_1 is directly connected to voltage source (V_i), and its current is linearly increased from its minimum value (I_{LV1}) to its maximum value (I_{LP1}). As a result, its stored energy is increased. During this time interval, the inductor L_2 and the capacitors C_1 and C_2 are in series and are connected to V_i. In this case, the current of inductor L_2 is linearly increased from its minimum (I_{LV2}) value to its maximum value (I_{LP2}). As a result, its stored energy is increased and the voltage of capacitor C_1 is decreased from its

maximum value (V_{CP1}) to its minimum value (V_{CV1}) and the voltage C_2 capacitor is increased from its minimum value (V_{CV2}) to its maximum value (V_{CP2}). Also, the voltage of capacitor C_3 is decreased from its maximum value (V_{CP3}) to its minimum value (V_{CV3}). The equivalent circuit of proposed converter in this time interval is shown in Fig. 2(a).

Mode II: In the first part of time interval of T_{off} (T'_{off}) in CCM and (t_1, t_2) in DCM when the switch S is turned off, the diodes of D_2 and D_3 are forward-biased and the diode D_1 is reverse-biased, the inductor L_1 is connected to the capacitor C_2, C_3 and load, as a result its current and stored energy are gradually decreased. Also, the inductor L_2 is connected to the capacitors C_1 and C_3 in series. Then, the current of inductor L_1 and its stored energy are gradually decreased to minimum value. During this time interval, the voltage of the capacitors C_1 and C_2 are decreased and the voltage of capacitor C_3 is gradually increased. The equivalent circuit of proposed converter in this time interval is shown in Fig. 2(b).

Mode III: In the second part of time interval of T_{off} (T''_{off}) in CCM and (t_2, t_3) in DCM, when the switch S is turned off and the diodes D_1, D_2 and D_3 are forward-biased, the current of the capacitor C_2 and inductor L_2 provide the charge current of capacitor C_3 and the load current; as a result, the voltage of capacitor C_2 and the current of inductor L_1 are reduced to their minimum values. Meanwhile, the stored energy of capacitor C_3 is increased to its maximum value, so its voltage reaches V_{CP3}. During this time interval, the capacitor C_1 is in parallel with the inductor L_1, thus its voltage is increased to its maximum value. In this case, the inductor L_1 current and its stored energy are reduced to their minimum values. Since the energy of load is provided by parallel path of L_1, L_2, C_1 and C_2, the inductors current is decreased to their minimum values at the same time. The equivalent circuit of proposed converter in this time interval is shown in Fig. 2(c).

Mode IV: At (t_3, t_4) in DCM when the switch S is turned off and the diodes D_1, D_2 and D_3 are reverse-biased, the current of the inductors L_1 and L_2 are zero and their stored energy are in their minimum values. Also, the voltage and stored energy of the capacitors C_1 and C_2 remain constant. During this time interval, the discharge current of capacitor C_3 provide the load current. As a result, its voltage and stored energy is decreased to their minimum values. The equivalent circuit of proposed converter in this time interval is shown in Fig. 2(d).

B. Analysis of Proposed Converter in CCM

By applying KVL in Fig. 2(a), we have:

$$v_{L1,1} = V_i = L_1 \frac{di_{L1,1}}{dt} = L_1 \frac{\Delta i_{L1}}{T_{on}} \quad (1)$$

where $v_{L1,1}$ and $i_{L1,1}$ denote the voltage and current of the inductor L_1 at T_{on}, respectively, and Δi_{L1} is its current ripple. By applying KVL in Figs. 2(b) and 2(c) at T_{off}, we would have:

$$v_{L1,3} = V_i + v_{C2,3} - v_{C3,3} = -v_{C1,3} = L_1 \frac{di_{L1,3}}{dt} = -L_1 \frac{\Delta i_{L1}}{T_{off}} \quad (2)$$

where $v_{L1,3}$, $v_{C1,3}$, $v_{C2,3}$ and $v_{C3,3}$ are the voltage of the inductor L_1 and capacitors C_1, C_2 and C_3 at T_{off}, respectively. $i_{L1,3}$ indicates the inductor L_1 current at T_{off}.

By substituting (1) and (2) into voltage-balancing rule of an inductor in steady state; considering Figs. 2(b) and 2(c), and assuming negligible value for T'_{off}, we have:

$$V_i T_{on} - v_{C1,3} T_{off} = 0 \quad (3)$$

where $v_{C1,3}$ represents the voltage of capacitor C_1 at T_{off}.

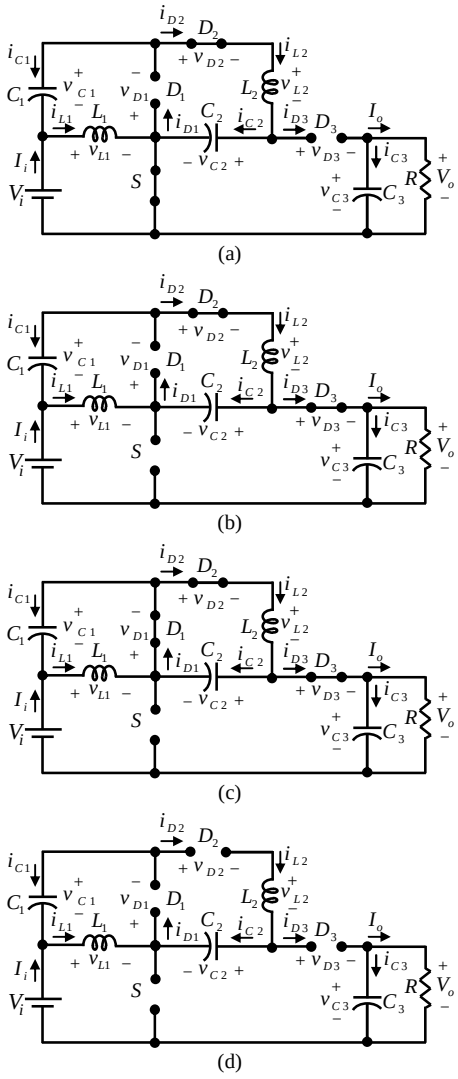

Fig. 2. Equivalent circuits of the proposed converter; (a) at T_{on} in CCM and (t_0, t_1) in DCM; (b) at T'_{off} in CCM and (t_1, t_2) in DCM; (c) at T''_{off} in CCM and (t_2, t_3) in DCM; (d) (t_3, t_4) in DCM

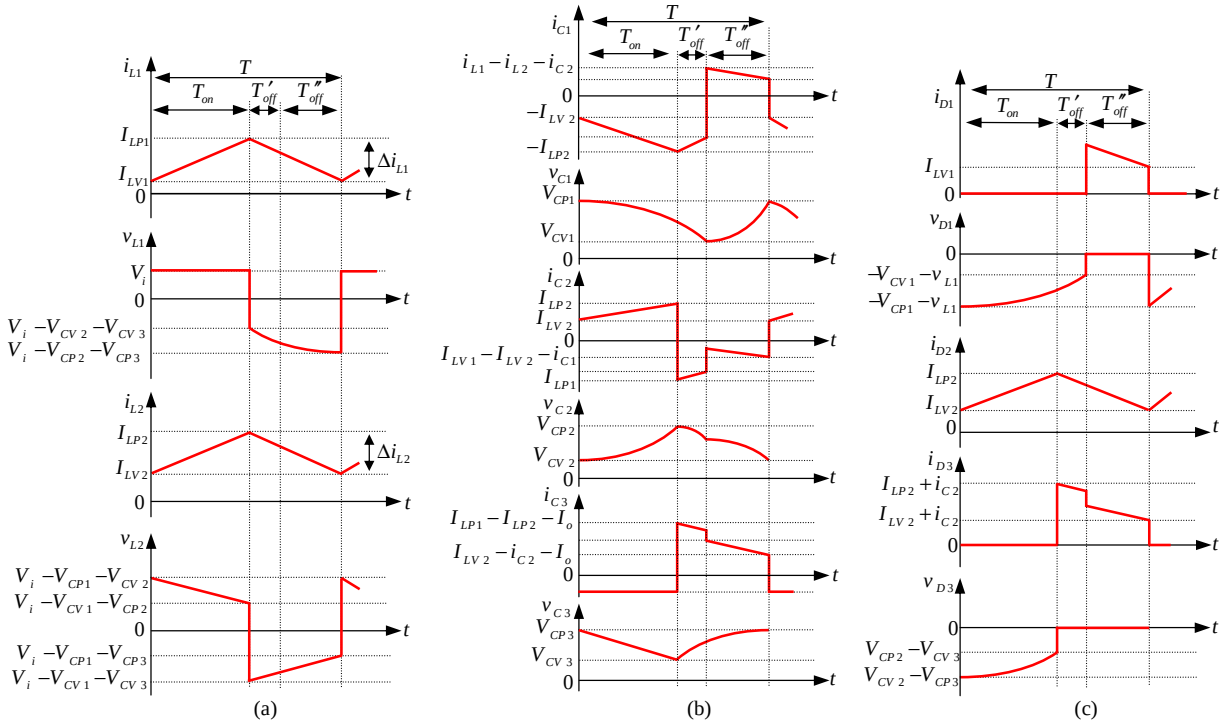

Fig. 3. Voltage and current waveforms in CCM for; (a) inductors L_1 and L_2; (b) capacitors C_1, C_2 and C_3; (c) diodes D_1, D_2 and D_3

By defining duty cycle of a dc-dc converter $(D = T_{on}/T)$, it is resulted:

$$v_{C1,3} = \frac{D}{1-D} V_i \tag{4}$$

From Fig. 2, we have:

$$v_{C1} = v_{C1,1} = v_{C1,2} = v_{C1,3} \tag{5}$$

where $v_{C1,1}$, $v_{C1,2}$ and v_{C1} are the voltage of capacitor C_1 at T_{on}, at T'_{off} and its average value in steady state, respectively.

The capacitor C_1 current at T_{on} $(i_{C1,1})$ is equal to:

$$i_{C1,1} = -i_{L2,1} = -i_{C2,1} \tag{6}$$

The capacitor C_1 current at T'_{off} $(i_{C1,2})$ is:

$$i_{C1,2} = -i_{L2,2} \tag{7}$$

The capacitor C_1 current at T''_{off} $(i_{C1,3})$ is equal to:

$$i_{C1,3} = i_{L1,3} - i_{L2,3} + i_{C2,3} \tag{8}$$

By applying KVL in Fig. 2(a), we have:

$$v_{L2,1} = V_i + v_{C1,1} - v_{C2,1} = L_2 \frac{di_{L2,1}}{dt} = L_2 \frac{\Delta i_{L2}}{T_{on}} \tag{9}$$

where $v_{L2,1}$ and $v_{C2,1}$ show the voltage of the inductor L_2 and capacitor C_2 at T_{on}, respectively. Also, $i_{L2,1}$ shows the inductor L_2 current at T_{on} and Δi_{L2} indicates its current ripple. By applying KVL in Figs. 2(b) and 2(c), we have:

$$v_{L2,3} = V_i + v_{C1,3} - v_{C3,3} = L_2 \frac{di_{L2,3}}{dt} = -L_2 \frac{\Delta i_{L2}}{T_{off}} \tag{10}$$

where $v_{L2,3}$ and $i_{L2,3}$ show the voltage and current of the inductor L_2 at T_{off}, respectively

By considering Fig. 2, we have:

$$v_{C1} = v_{C2} \tag{11}$$

where v_{C2} represents the average voltage of capacitor C_2.

The capacitor C_2 current at T_{on} $(i_{C2,1})$ is as follows:

$$i_{C2,1} = i_{L2,1} \tag{12}$$

From Fig. 2(b), the capacitor C_2 current $(i_{C2,2})$ is equal to:

$$i_{C2,2} = -i_{L1,2} \tag{13}$$

where $i_{L1,2}$ represents the inductor L_1 at T'_{off}.

The below relation is obtained for the capacitor C_2 current at T''_{off} $(i_{C2,3})$ as follows:

$$i_{C2,3} = i_{L1,3} - i_{C1,3} - i_{L2,3} \tag{14}$$

According to Fig. 2, the average voltage of capacitor C_3 (v_{C3}) is equal to:

$$v_{C3} = V_o \tag{15}$$

The capacitors C_3 currents at T_{on} $(i_{C3,1})$, at T'_{off} $(i_{C3,2})$ and at T''_{off} $(i_{C3,3})$ are , respectively:

$$i_{C3,1} = -I_o \tag{16}$$

$$i_{C3,2} = i_{L1,2} + i_{L2,2} - I_o \tag{17}$$

$$i_{C3,3} = i_{L2,3} - i_{C2,3} - I_o \tag{18}$$

where I_o represents the average load current.

According to Fig. 2, the voltages of diode D_1 at T_{on} $(v_{D1,1})$ and at T'_{off} $(v_{D1,2})$ are respectively equal to:

$$v_{D1,1} = -v_{C1,1} - v_{L1,1} \tag{19}$$

$$v_{D1,2} = -v_{C1,2} - v_{L1,2} \tag{20}$$

From Fig. 2(c), the current of diode D_1 at T_{off}'' ($i_{D1,3}$) is extracted as follows:

$$i_{D1,3} = i_{L2,3} + i_{C1,3} \quad (21)$$

The current relation of diode D_2 (i_{D2}) is obtained as:

$$i_{D2} = i_{L2} \quad (22)$$

The voltage of diode D_3 at T_{on} ($v_{D3,1}$) and its current at T_{off} ($i_{D3,3}$) respectively are:

$$v_{D3,1} = v_{C2,1} - v_{C3,1} \quad (23)$$

$$i_{D3,3} = i_{L2,3} + i_{C2,3} \quad (24)$$

By applying voltage-balancing rule for L_2 in steady state and replacing (9) and (10) into it, the proposed boost converter voltage gain in CCM is obtained as follows:

$$\frac{V_o}{V_i} = \frac{1+D}{1-D} \quad (25)$$

Assuming no losses, it is resulted:

$$\frac{I_o}{I_i} = \frac{1-D}{1+D} \quad (26)$$

where I_i is the average input current.

Assuming pure resistance load (R) and taking into account (25) and (26), we have the following equation:

$$I_i = \frac{(1+D)^2}{(1-D)^2}\frac{V_i}{R} \quad (27)$$

Summary results of the comparison between the proposed converter and other boost converters are presented in Table I. Also, by assuming the same input voltage, the efficiency variation analysis has been done between the proposed converter and presented converter in [28] and [29], and its curve is shown in Fig. 4. As shown in Fig. 4, the proposed converter in [28] provided the lowest efficiency whereas the proposed converter and presented in [29] have acceptable efficiency in compression with the presented converter in [28]. Of course, the proposed converter efficiency is higher than other presented converters in [28] and [29] for some duty cycles. On the other hand, higher and more acceptable voltage gain is provided by the proposed converter with less elements and switches than other presented converters. For more details, the proposed converter and presented converter in [11] have been introduced by different techniques; however one less diode and capacitor is used in the structure of the proposed converter in compression with that of [11]. Additionally, the controlling of switches in [11] was done by phase difference and, unlike proposed converter; the output capacitor consists of two series capacitors witch common middle point. Most importantly, the duty cycle ratio of presented converter in [11] was limited to less than 0.5 in practice as a result the output voltage gain ratio was limited.

C. Analysis of Proposed Converter in DCM

By applying KVL in Fig. 2(a), we have:

$$v_{L1,1} = V_i = L_1\frac{i_{L1,1}}{dt} = L_1\frac{\Delta i_{L1}}{\Delta t} \quad (28)$$

where $v_{L1,1}$ and $i_{L1,1}$ indicate the voltage and current of the inductor L_1 at (t_0, t_1), respectively, and Δi_{L1} shows its current ripple. By applying KVL in the circuit shown in Figs. 2(c) and 2(d), we have:

$$v_{L1,3} = V_i + v_{C2,3} - v_{C3,3} = L_1\frac{di_{L1,3}}{dt} = -L_1\frac{\Delta i_{L1}}{\Delta t} \quad (29)$$

where $v_{L1,3}$, $v_{C2,3}$ and $v_{C3,3}$ indicate the voltage of the inductor L_1, capacitors C_2 and C_3 at (t_1, t_3), respectively. Also, $i_{L1,3}$ shows the inductor L_1 current at (t_1, t_3).

The current and voltage of the inductor L_1 at (t_3, t_4) ($i_{L1,4}$) ($v_{L1,4}$) is as follows:

$$i_{L1,4} = 0 \quad (30)$$

$$v_{L1,4} = 0 \quad (31)$$

The following equations are defined for time intervals in DCM:

$$D_1' = \frac{t_0 - t_1}{T} \quad (32)$$

$$D_2' = \frac{t_2 - t_1}{T} \quad (33)$$

$$D_3' = \frac{t_3 - t_2}{T} \quad (34)$$

$$D_4' = \frac{t_4 - t_3}{T} \quad (35)$$

where D_1' is the duty cycle of proposed converter in DCM.

TABLE I
COMPARISON BETWEEN DIFFERENT BOOST CONVERTRES

Element number/Converter	Switch	Inductor	Capacitor	Diode	Voltage gain in CCM
Conventional boost converter	1	1	1	1	$\frac{1}{1-D}$
Presented in [11]	2	2	4	4	$\frac{4}{1-D}$
Presented in [13]	8	4	4	-	$\frac{2n}{1-D}$
Presented in [16]	1	2	2	3	$\frac{1}{(1-D)^2}$
Presented in [20]	2	2	4	4	$\frac{4}{1-D}$
Presented in [27]	2	3	4	3	$\frac{2}{1-D}$
Presented in [29]	2	3	3	4	$\frac{2}{D(1-D)}$
Proposed topology	1	2	3	3	$\frac{1+D}{1-D}$

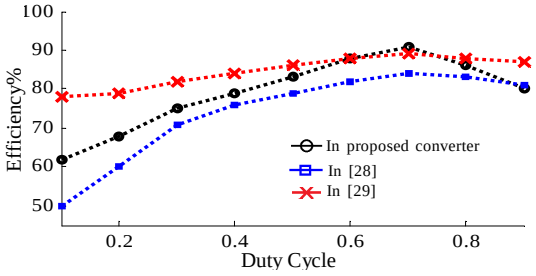

Fig. 4. Efficiency compression between different converters for versus duty ratios

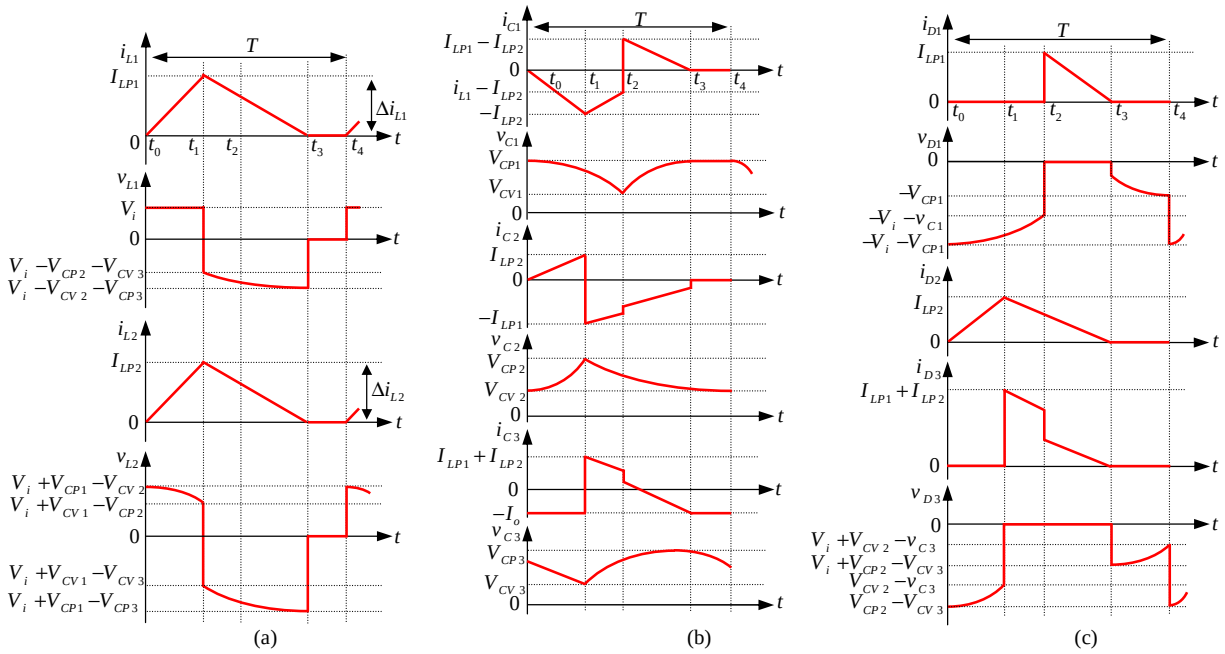

Fig. 5. Voltage and current waveforms in DCM for; (a) inductors L_1 and L_2; (b) capacitors C_1, C_2 and C_3; (c) diodes D_1, D_2 and D_3

By applying voltage-balancing rule for inductor L_1 and substituting (28), (29) and (31), the following is obtained:

$$v_{C2,3} = \frac{D_1'}{D_4'} V_i = v_{C2} = v_{C2,1} = v_{C2,2} = v_{C2,4} \tag{36}$$

where $v_{C2,1}$ and $v_{C2,4}$ indicate the voltage of capacitor C_2 at $(t_0,\ t_1)$ and $(t_3,\ t_4)$, respectively, and v_{C2} is the capacitor C_2 average voltage. According to Fig. 2(c), the current of capacitor C_2 at $(t_0,\ t_1)$ $(i_{C2,1})$ is equal to:

$$i_{C2,1} = i_{L2,1} \tag{37}$$

where $i_{L2,1}$ shows the inductor L_2 current at $(t_0,\ t_1)$.

According to Figs. 2(c) and 2(d), the capacitor C_2 current at $(t_1,\ t_2)$, $(i_{C2,2})$, and $(t_2,\ t_3)$, $(i_{C2,3})$ are equal to:

$$i_{C2,2} = -i_{L1,2} \tag{38}$$

$$i_{C2,3} = i_{L2,3} + i_{C1,3} - i_{L1,3} \tag{39}$$

where $i_{L2,3}$ and $i_{C1,3}$ represent the current of the inductor L_2 and capacitor C_1 at $(t_2,\ t_3)$, respectively. By applying KVL in the circuit of Fig. 2(a), we would have:

$$v_{L2,1} = V_i + v_{C1,1} - v_{C2,1} = L_2 \frac{di_{L2,1}}{dt} = L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{40}$$

where $v_{L2,1}$ and $v_{C1,1}$ indicate the voltage of the inductor L_2 and capacitor C_1 at $(t_0,\ t_1)$, respectively. Δi_{L2} shows the inductor L_2 ripple current.

By applying KVL in Fig. 2(c), it is resulted:

$$v_{L2,3} = V_i + v_{C1,3} - v_{C3,3} = L_2 \frac{di_{L2,3}}{dt} = -L_2 \frac{\Delta i_{L2}}{\Delta t} \tag{41}$$

where $v_{L2,3}$ and $v_{C1,3}$ indicate the voltage of the inductor L_2 and capacitor C_1 at $(t_1,\ t_3)$, respectively. $i_{L2,3}$ shows the inductor L_2 current at $(t_1,\ t_3)$. By applying KVL in Figs. 2(d) and 2(e), the inductor L_2 current at $(t_3,\ t_4)$ $(i_{L2,4})$ and its voltage $(v_{L2,4})$ are obtained as follows, respectively:

$$i_{L2,4} = 0 \tag{42}$$

$$v_{L2,4} = 0 \tag{43}$$

By substituting (32) into (35) and (36) and considering large capacitance for capacitor C_1, the average voltage of capacitor C_1 (v_{C1}) is equal to:

$$v_{C1} = \frac{D_1'}{1-(D_1'+D_2')} V_i = v_{C1,1} = v_{C1,2} = v_{C1,3} = v_{C1,4} \tag{44}$$

where $v_{C1,3}$ and $v_{C1,4}$ are the voltage of capacitor C_1 at $(t_2,\ t_3)$ and $(t_3,\ t_4)$, respectively.

The voltage of capacitor C_1 at $(t_0,\ t_2)$ $(i_{C1,2})$ is as:

$$i_{C1,2} = -i_{L2,2} \tag{45}$$

At $(t_2,\ t_3)$, the voltage of capacitor C_1 $(i_{C1,3})$ is as:

$$i_{C1,3} = i_{L1,3} - i_{L2,3} + i_{C2,3} \tag{46}$$

From Fig. 2, we would have the following equation for output voltage (V_o):

$$v_{C3} = V_o \tag{47}$$

From Figs. 2(a) and 2(e), the current of capacitor C_3 at $(t_3,\ t_1)$ is as follows:

$$i_{C3,1} = -I_o \tag{48}$$

From Figs. 2(c) and 2(d), the following relation is obtained for the current of capacitor C_3 at $(t_1,\ t_3)$:

$$i_{C3,3} = i_{L1,3} + i_{L2,3} - I_o \tag{49}$$

The voltage of diode D_1 at $(t_0,\ t_2)$ $(v_{D1,2})$ is as follows:

$$v_{D1,2} = -(v_{L1,2} + v_{C1,2}) \tag{50}$$

The voltage of diode D_1 at $(t_3,\ t_4)$ $(v_{D1,4})$ is as follows:

$$v_{D1,4} = -v_{C1,4} \tag{51}$$

The current of diode D_1 at $(t_2,\ t_3)$ $(i_{D1,3})$ is expressed as:

$$i_{D1,3} = i_{L1,3} - i_{C2,3} \tag{52}$$

At $(t_0,\ t_3)$, the following relation is achieved for the current of diode D_2 $(i_{D2,3})$:

$$i_{D2,3} = i_{L2,3} \tag{53}$$

The voltage of diode D_3 at $(t_0,\ t_1)$ $(v_{D3,1})$ is achieved as:

$$v_{D3,1} = v_{C2,1} - v_{C3,1} \tag{54}$$

The current of diode D_3 at $(t_1,\ t_3)$ $(i_{D3,3})$ is obtained as:

$$i_{D3,3} = i_{L2,3} - i_{C2,3} \tag{55}$$

The below relation is obtained for the diode D_3 voltage at $(t_3,\ t_4)$ $(v_{D3,4})$:

$$v_{D3,4} = V_i + v_{C2,4} - v_{C3,4} \tag{56}$$

By applying voltage-balancing rule for inductor L_2 and substituting (40), (41) and (43), the proposed converter voltage gain in DCM is calculated as follows:

$$\frac{V_o}{V_i} = \frac{1+D_1'}{D_2'+D_3'} \tag{57}$$

Assuming no losses, it is concluded that:

$$\frac{I_o}{I_i} = \frac{D_2'+D_3'}{1+D_1'} \tag{58}$$

For pure resistance load (R), we get:

$$I_i = \frac{(1+D_1')^2}{(D_2'+D_3')^2}\frac{V_i}{R} \tag{59}$$

III. Critical Inductance Calculation

By considering $I_{LV1} + I_{LV2} = 0$ we get in critical mode, and to calculate the critical inductances of L_1, L_{C1}, and L_2, L_{C2}, the current-balancing rule in CCM mode for capacitor C_3 and substituting (16), (17) and (18) into it, it is concluded that:

$$I_{LP1} = \frac{V_i DT}{2L_1} + \frac{I_o}{(1-D)^2} - \frac{V_i D}{2L_1 I_o (1-D)^2}\left(\frac{1+D}{1-D}\right)^2 T^2 \tag{60}$$

From (25) and (60), and considering $I_{LV1} = 0$, the below relation is achieved for L_{C1}:

$$L_{C1} = \frac{1}{2}\left(\frac{D(1-D)^3}{1+D} + \frac{RD}{f}\right)\frac{R}{f} \tag{61}$$

where it can be noted that L_{C1} depends on D, R and f.

By applying current-balancing rule for capacitor C_1 in CCM mode, and by substituting (6), (7) and (8) into it and ignoring T_{off}', we get:

$$I_{LP2} = -\frac{V_i D(1-D)T}{2L_2} + \frac{V_i}{2L_2}\frac{D^3(1-D)T}{(1+D)} - \frac{I_o}{R(1+D)} + \frac{V_i}{2L_2}\frac{D^3RT^2}{(1-D)} + \frac{V_i}{2L_2}\frac{D(1+D)}{(1-D)}RT^2 \tag{62}$$

From (26) and (62), the following can be obtained for L_{C2}:

$$L_{C2} = \frac{1}{2}\left(\frac{D(1-D)^3}{1+D} + \frac{RD}{f}\right)\left(\frac{D^2}{1-D} + \frac{1+D}{1-D}\right)\frac{R}{f} \tag{63}$$

From the above equation, it can be concluded that L_{C2} depends on D, R and f.

The normalized magnetizing inductor time constant can be defined as $\tau_L = 2L_e f / R$ where $L_e = L_1 \| L_2$. When the proposed converter is operating in critical mode, the CCM and DCM voltage gains are equal. Using (25) and (57), the following equation is obtained as critical normalized magnetizing inductor time constant τ_{Cri}:

$$\tau_{Cri} = \frac{9D^2(1-D)^2}{8(1+D)^2} = \frac{9D^2}{8}\left(\frac{V_i}{V_o}\right)^2 \tag{64}$$

From (64), if $\tau_L > \tau_{Cri}$ proposed converter operates as CCM, otherwise it operates as DCM.

IV. Switching Stress Calculation

By selecting the appropriate switching, the cost of a converter can be reduced to the minimum. One of the main criteria for selecting the type of switch is peak current flow switch (PCFS). In this section, equations related to current of switches are calculated for CCM and DCM.

A. Calculation of PCFS in CCM

According to Fig. 2(a), the switch S current (i_S) is:

$$i_S = i_{L1,1} + i_{L2,1} \tag{65}$$

At $t = T_{on}$, the current of switch S is increased to its maximum value (i_{SP}^{CCM}) and is calculated as follows:

$$i_{SP}^{CCM} = I_{LP1} + I_{LP2} \tag{66}$$

According to above equation it is clear that i_{SP}^{CCM} value has inverse relation with L_1 and L_2, and direct relation with R. By substituting $L_1 = L_{C1}$ and $L_2 = L_{C2}$, the value of i_{SP}^{CCM} is increased to its maximum value $(i_{SP,\max}^{CCM})$. By substituting (61) and (63) into (66), the following is obtained for $i_{SP,\max}^{CCM}$:

$$\begin{aligned} i_{SP,\max}^{CCM} = {} & \frac{V_i^2 D^2}{V_o\left(\frac{(1-D)^3}{1+D}+RT\right)\left(\frac{D}{1-D}+\frac{1+D}{D(1-D)}\right)R} - \frac{I_o}{R(1+D)} \\ & - \frac{V_i(1-D)}{\left(\frac{(1-D)^3}{1+D}+RT\right)\left(\frac{D}{1-D}+\frac{1+D}{D(1-D)}\right)R} + \frac{V_i}{\left(\frac{(1-D)^3}{1+D}+RT\right)R} \\ & + \frac{V_o T}{\left(\frac{(1-D)^3}{1+D}+RT\right)\left(\frac{D}{1-D}+\frac{1+D}{D(1-D)}\right)} - \frac{V_o T}{V_i(1-D)^2\left(\frac{(1-D)^3}{1+D}+RT\right)} \\ & + \frac{V_i D^2 T}{(1-D)\left(\frac{(1-D)^3}{1+D}+RT\right)\left(\frac{D^2}{1-D}+\frac{1+D}{1-D}\right)} + \frac{I_o}{(1-D)^2} \end{aligned} \tag{67}$$

B. Calculation of PCFS in DCM

According to Fig. 2(a), i_S in DCM mode is as follows:

$$i_S = i_{L1,1} + i_{L2,1} \tag{68}$$

At $t = t_1$, the switch S current reaches its maximum value (i_{SP}^{DCM}). We get the following equation:

$$i_{SP}^{DCM} = I_{LP1} + I_{LP2} \tag{69}$$

V. Efficiency Analysis

It can be noted the ripples of inductors and capacitors are neglected for efficiency analysis of the proposed converter. During this analysis, the switch on-state resistance is defined as r_S, the forward resistance of D_1, D_2 and D_3 diodes are defined as r_{D1}, r_{D2} and r_{D3}, respectively. Also, the threshold voltages of D_1, D_2 and D_3 diodes are considered as V_{F1}, V_{F2} and V_{F3}, respectively. Meanwhile, r_{L1} and r_{L2} are the equivalent series resistance (ESR) of inductors L_1 and L_2, respectively. In addition, r_{C1}, r_{C2} and r_{C3} are the ESR of capacitors C_1, C_2 and C_3, respectively. Then, the resistance loss of the diodes is obtained as follows:

$$P_{rD} = r_{D1}\frac{(1+D)^2}{D}I_o^2 + r_{D2}\frac{(1+D)^2}{D}I_o^2 + r_{D3}\frac{(1+D)^2}{D}I_o^2 \tag{70}$$

The below relation is extracted to the threshold voltage losses of diodes:

$$P_{F,D} = V_{F1}\frac{1+D}{1-D}I_o + V_{F2}I_o + V_{F3}I_o \tag{71}$$

The resistance losses of inductors and capacitors are obtained as follows, respectively:

$$P_{rL} = r_{rL1}\left(\frac{1+D}{1-D}\right)^2 I_o^2 + r_{rL2}I_o^2 \tag{72}$$

$$P_{rC} = r_{rC1}\frac{1+D}{D}I_o^2 + r_{rC2}\frac{1+D}{D}I_o^2 + r_{rC3}\frac{(1+D)^2}{R^2}V_i \tag{73}$$

The switch losses can be extracted as follows:

$$P_S = r_{rS}\frac{1+D}{1-D}I_o + \frac{D(1+D)}{(1-D)^2}V_i I_o \tag{74}$$

The switching losses of switch and diodes are calculated as follows:

$$P_{S,switching} = \frac{1+D}{6(1-D)^2}V_i I_o\left[\frac{t_{on,s}+t_{off,s}}{T}\right] \tag{75}$$

$$P_{D,switching} = \frac{(1+D)V_i I_o}{6(1-D)\sqrt{D}}\left[\frac{t_{on,D1}+t_{off,D1}+t_{on,D3}+t_{off,D3}}{T}\right] \tag{76}$$

where $t_{on,s}$, $t_{off,s}$, $t_{on,D1}$, $t_{off,D1}$, $t_{on,D3}$ and $t_{off,D3}$ are the characterizes of switch and diodes. Note that the switching loss of D_2 diode can be neglected due to its off-state voltage value. Using (70)-(74) and considering switch losses as P_{Switch}, the efficiency of proposed converter is obtained as follows:

$$\eta\% = \frac{1}{1+\dfrac{P_{rD}+P_{F,D}+P_{rL}+P_{rC}+P_{Switch}+P_{S,Switching}+P_{D,Switching}}{P_o}}\times 100 \tag{77}$$

VI. Experimental Results

To verify the extracted theoretical concepts of the proposed converter, the experimental results are obtained at CCM and DCM. These results are obtained under presented parameters in Table II. Meanwhile, the parameters of the proposed converter prototype are presented in Table III.

TABLE II
ANALYSIS PARAMETERS

Parameters	CCM	DCM	Parameters	CCM	DCM
Duty cycle	$D=50\%$	$D'=50\%$	$C_1=C_2$	$110\mu F$	
L_1	$5mH$	$100\mu H$	C_3	$63\mu F$	
L_2	$2mH$	$500\mu H$	V_i	$12V$	
R	100Ω		f	$10kHz$	

TABLE III
PARASITIC PARAMETERS OF CONVERTER FOR LABORATORY PROTOTYPE

Parameters	Value	Parameters	Value
r_{L1}	$20m\Omega$	r_{C3}	$10m\Omega$
r_{L2}	$15m\Omega$	D_1 to D_3	$V_F=1V$ / $r_D=10m\Omega$
$r_{C1}=r_{C2}$	$15m\Omega$	Switch	$V_F=1V$ / $r_S=10m\Omega$

A. Critical Inductance Calculation

Considering Table II and applying (61) and (63), the values of L_{C1} and L_{C2} are $233\mu H$ and $810\mu H$, respectively. Considering L_{C1} and L_{C2}, the proposed converter would be in critical mode. For $L_1 > L_{C1}$ and $L_2 > L_{C2}$, the proposed converter would operate in CCM and for $L_1 < L_{C1}$ and $L_2 < L_{C2}$, the proposed converter would operate in DCM. Considering critical inductance values, the current value of switch S in accordance (67) is equals to $3.2A$.

B. Experimental Results for CCM

In order to verify the satisfying operation of proposed converter, a laboratory prototype is built. The operating of proposed converter is examined under CCM at $D = 50\%$. The other parameters of the implemented circuit are presented in Tables 2 and 3. The experimental results are shown in Fig. 6. The inductors voltage confirms the theoretical concepts. As shown in Figs. 6(a) and 6(b), the voltage of the inductors L_1 and L_2 are increased at T_{on} and in accordance with (1) and (9) both are approximately $12V$. In addition, the voltage of the inductors L_1 and L_2 are decreased during T_{off} in accordance with (2) and (10), respectively.

The voltage waveforms of the capacitors C_1 and C_3 are shown in Figs. 6(c) and 6(d), respectively. It is obvious that $v_{C1} = 12V$. Using (15) and (25), the theoretical value of average load voltage is 36V, which is verified by presented results in Fig. 6(d). It should be noted that there are differences between theoretical and experimental results due to parasitic components. The performance of the proposed converter under different load and step load is shown in Fig. 7(a). It is assumed that the load value changes from 100Ω to 10Ω and then 500Ω at $t = 0.15S$ and $t = 0.30S$, respectively. As it can be seen, the load voltage can reach to its steady state with small ripple due to considering limited capacitance for output capacitor when load is varied. Low

time constant for output capacitor discharging is occurred when the light load is considered, as a result, the energy of capacitor C_3 is discharged at the load and the output voltage is reduced. But, in the large resistive load, given that the time constant of capacitor discharge is increased then the energy of the capacitor is reduced less. The time constant variations of capacitor discharge in the different loads are caused a slight ripple in the amount of the output voltage at steady state. Of course, the output voltage can be fixed in steady state for different loads by designing proposer closed-loop control system. The efficiency analysis of proposed converter is shown in Fig. 7(b) under same V_i and D, and different loads. As illustrated, the highest calculated efficiency in simulation is approximately 96%, while the highest calculated efficiency is almost 93.8%. Meanwhile, the switch S current in CCM is changed in accordance with (65) and its maximum value is achieved at $t = T_{on}$ to $1.7A$ (eq. (66)).

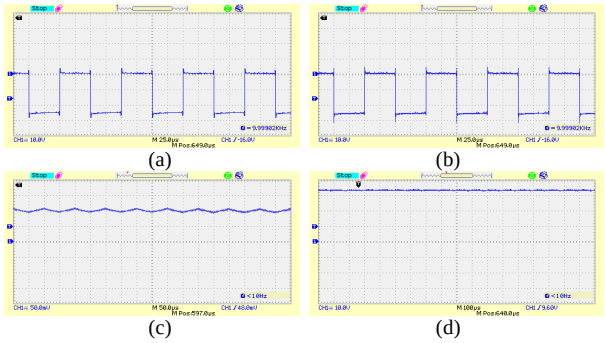

Fig. 6. Experimental results in CCM for; (a) L_1 voltage; (b) L_2 voltage; (c) C_1 voltage; (d) C_3 voltage

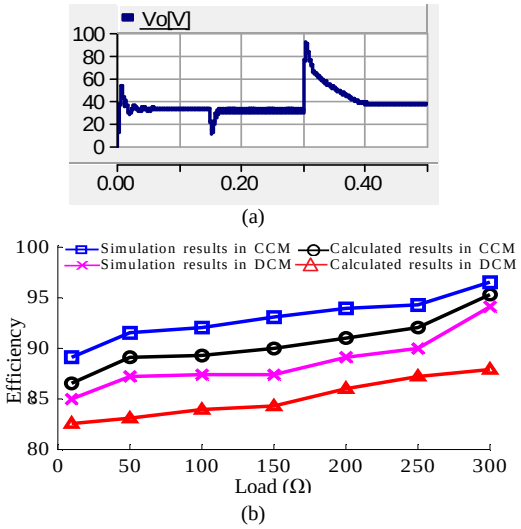

Fig. 7. (a) The output voltage variations by load changing; (b) Efficiency analysis of the proposed converter

C. Experimental Results for DCM

Considering Table II, the proposed converter would be in DCM. The experimental results in this mode are shown in Fig. 8. As shown in Figs. 8(a) and 8(b), the voltage of inductor L_1 is in accordance with (28), (29) and (31). Also, the voltage of inductor L_2 is in accordance with (40), (41) and (43). The voltage of the capacitors C_1 and C_3 are shown in Figs. 8(c) and 8(d), respectively. It is obvious that $v_{C1} = 20V$, in accordance with (66). The average voltage of the capacitor C_3 and load is $52.5V$, in accordance with (47) and (57), respectively. It can be noted that the differences between theoretical and experimental results are due to parasitic components. As shown in Fig. 7(b), the highest efficiency values of proposed converter in simulation and calculated are approximately 90.5% and 87.9%, respectively. Also, the switch S current is equals to $7A$ in accordance with (69) at DCM.

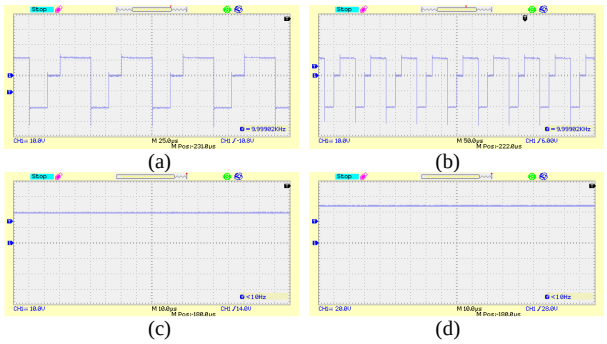

Fig. 8. Experimental results in DCM for; (a) L_1 voltage; (b) L_2 voltage; (c) C_1 voltage; (d) C_3 voltage

VII. Conclusion

In this paper, a new structure for non-isolated dc-dc boost converters was proposed by VL technique and its voltage and current equations of elements and semiconductor devices were extracted in CCM and DCM, and critical inductance relations were calculated. Following, the structure of proposed converter and its efficiency was compared in CCM with other conventional non-isolated boost converters from the standpoint of number of switches, inductors, capacitors and diodes, and voltage gain at CCM. It was shown that for same inputs, the proposed converter provided higher voltage gain. Considering $V_i = 12V$, $f = 10kHz$, $D = 50\%$ and $D' = 50\%$, the average load voltage in CCM and DCM are $36V$ and $52.5V$, respectively, which the theoretical and experimental results confirm fairly each other. Given that these voltage gains achieved just by only one switch which turned on and turned off by specified duty cycle (dependent on voltage gain) then special controller system is not required. In addition, the current stress of switch was studied. The PCFS of switch S in CCM, critical and DCM are $1.7A$, $3.2A$ and $7A$, respectively.

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