A ZCS-PWM Interleaved Boost Rectifier

Chien-Ming Wang, Chien-Ju Lin, and Kuan-Yu Chen
Department of Electrical Engineering
National Ilan University
I-Lan, Taiwan

Abstract—A ZCS-PWM interleaved boost rectifier with high power factor is proposed in this paper. The pulse-width-modulation technique and soft commutation technique are used in the proposed rectifier to promote the circuit performance. The proposed circuit includes two boost converters which are operated at interleaved mode to increase the output power and reduce the input ripple current. A ZCS-PWM auxiliary circuit is configured in the presented rectifier to provide the ZCS function on main switches and auxiliary switches and improve the problem of switching losses and EMI. A prototype has been implemented in laboratory to verify circuit theory.

Keywords—dc power supply system; ZCS-PWM

I. INTRODUCTION

The power source of the electronic products is dc power source. A full-bridge diode rectifier with a large filter capacitor as the front-end rectification is a popularly conventional method to get dc voltage. However, it will encounter excessive peak input current and high harmonic distortion. The power factor is low and is about 0.5-0.6. How to reduce input current harmonics and enhance input power factor is important topic. Adopting a power factor correction (PFC) circuit in the dc power supply is the most popular method. The passive power factor corrector which composes of inductors and capacitors is an early method. This method can increase the power factor above 0.8. However, the volume and weight of the circuit are larger. It is not conformed the required size of portable the electronic products. The active power factor correction circuit is used to improve this problem in recent year. The boost power factor corrector with high power factor and low inductor ripple current is the most general used circuit [1]-[4]. For increasing the rated output power, it must employ more this converter in parallel. This solution will result in that the switching noise interferes with each other because they are asynchronous operation. The interleaving operation methods can be used to improve this problem [5]-[9]. It can promote PFC performance and reduced size of PFC. Besides, each converter can share the total power to enable the current through the main switches is only fraction of the total input current. The interleaving operation method can control the interleaved phase to cancel partial input ripple current. This circuit must be operated at high switching frequency for getting high power density. Unfortunately, it will result in higher switching losses and electromagnetic interference noises. In order to improve this problem, many researches of soft-switching technique in interleaving boost PFC circuit have been done [10]-[11].

A ZCS-PWM interleaved boost rectifier with a ZCS-PWM auxiliary circuit by the similar concept is presented in this paper. The proposed rectifier is shown in Fig. 1(b). The proposed rectifier only uses a simple auxiliary circuit. Thus, the circuit complexity and cost are lower. It can provide the ZCS characteristic on main switches and auxiliary switches to improve the problem of switching losses and EMI. Besides operating at constant frequency and reducing commutation losses. Its configuration is inherently simple and compact. A design example are described and verified by experimental results from the 1kW prototype rectifier.

Fig. 1 (a) Circuit topology of the interleaved boost rectifier. (b) Circuit topology of the proposed ZCS-PWM interleaved boost rectifier.

II. PRINCIPLE OF PROPOSED ZCS-PWM INTERLEAVED BOOST RECTIFIER

The power stage diagram of the proposed ZCS-PWM interleaved boost rectifier is shown in Fig. 1(b). The circuit can be divided in two sections. The first section is a conventional interleaved boost rectifier. It is composed of input inductors $L_{in1}$, $L_{in2}$, switches $S_1$, $S_2$, diodes $D_1$, $D_2$, and output filter capacitor $C_o$. This section performs the operation of conventional interleaved boost rectifier. The second section is a ZCS-PWM auxiliary circuit to provide the zero-current-switching on the switches $S_1$, $S_2$, and diodes $D_1$, $D_2$. It is composed of the auxiliary diodes $D_{a1}$, $D_{a2}$, the resonant inductors $L_{r1}$, $L_{r2}$, $L_{r3}$, the resonant capacitor $C_r$, and auxiliary switch $S_a$ which are rated for a small power when compared to the output power. In proposed interleaved boost rectifier circuit, the circuit operation in positive half cycle of input line voltage is the same as one in negative half cycle of input line voltage. To simplify the analysis, the circuit operation in positive half cycle of input line voltage is only described in this paper. Because the proposed circuit is focused on higher boost conversion ratio application, the duty cycle is larger than 0.5. It is operated at CCM. It is assumed that the rectifier is operating in steady-state. And the following assumptions are made during one switching cycle.

1. All components and devices are ideal.
2. The inductors $L_{in1}$ and $L_{in2}$ are large enough to assume that the current $i_{in1}$ and $i_{in2}$ are constant and are much greater than resonant inductors $L_{r1}$, $L_{r2}$, $L_{r3}$.
3. The capacitor $C_o$ is large enough to assume that the voltage $V_o$ is constant and ripple free.
4. Input voltage $V_{in}$ is constant.
5. The voltage of resonant capacitor $C_r$ equals zero, and the resonant currents of the resonant inductors equal zero.

Based on these assumptions, circuit operations in one switching cycle can be divided into sixteen stages. The sixteen dynamic equivalent circuits of the ZCS-PWM interleaved boost rectifier during one switching period are shown in Fig. 2. The ideal relevant waveforms of proposed ZCS-PWM interleaved boost rectifier are shown in Fig. 3.

**STAGE 1:** $[t_0, t_1]$, Fig. 2(a).

Before $t=t_0$, the main switch $S_1$ maintains turn-off state and the main switch $S_2$ maintains turn-on state, the energy stored inductor $L_{in1}$ is delivered to output port through $D_1$. The inductor $L_{in2}$ and $L_r$ are charged by DC source $V_{in}$. This stage begins when $S_1$ turns on with ZCS. The resonant inductor $L_r$ charges linearly by output voltage $V_o$ from zero to $I_{in1}$. The stage ends when the resonant current $i_{Lr1}(t)$ reaches $I_{in1}$ and diode $D_1$ turns off with ZCS.

**STAGE 2:** $[t_1, t_2]$, Fig. 2(b).

In this stage, the inductors $L_{in1}, L_{in2}$ are charged by DC source $V_{in}$. The other semiconductors are in the off state.

**STAGE 3:** $[t_2, t_3]$, Fig. 2(c).

In this stage, the resonance begins when $S_1$ turns on with ZCS. The resonant route proceeds by way of $V_o, C_r, L_r$, and $S_1$. The resonant current $i_{Lr1}(t)$ increases and then decreases when arrive its peak value. The resonant voltage $v_{Cr}(t)$ also increases. This state is end when the resonant current $i_{Lr1}(t)$ drops to null again.

**STAGE 4:** $[t_3, t_4]$, Fig. 2(d).

During this stage, the auxiliary circuit performs continuously resonance operation. But, the resonant route is changed to the way of $V_o, C_r, L_{in1}, L_{in2}, D_{a1}, D_{a2}, S_1$, and $S_2$. Resonant capacitor $C_r$ is discharged through $S_1$ and $S_2$. The resonant voltage $v_{Cr}(t)$ decreases and resonant currents $i_{Lr1}(t)$, $i_{Lr2}(t)$ decrease via the resonance of $L_{in1}, L_{in2}$, and $C_r$. This state ends when the resonant currents $i_{Lr1}(t), i_{Lr2}(t)$ drop to zero.

**STAGE 5:** $[t_4, t_5]$, Fig. 2(e).

In this stage, the input current $I_{in1}$ flows through $D_{a1}, C_r$ and $V_o$. And, the input current $I_{in2}$ flows through $D_{a2}, C_r$ and $V_o$. Therefore, $v_{Cr}(t)$ decreases linearly toward $V_o$ which reached $V_o$ at the instant $t=t_5$.

**STAGE 6:** $[t_5, t_6]$, Fig. 2(f).

In this stage, the resonance begins again. The resonant route proceeds by way of $V_o, C_r, D_{a1}, L_{in1}$, and $S_1$. The resonant current $i_{Lr1}(t)$ increases and $V_o$ and resonant voltage $v_{Cr}(t)$ decreases. This state is end when the resonant current $i_{Lr1}(t)$ reached $I_{in1}$.

**STAGE 7:** $[t_6, t_7]$, Fig. 2(g).
In this stage, the input current $i_{in2}$ flows through $D_{a2}$, $C_r$, and $V_o$. Therefore, $v_{C}(t)$ decreases linearly toward zero, which reached at the instant $t=t_z$.

**STAGE 8: $[t_z, t_9]$**, Fig. 2(h).

In this stage, the input inductor $L_{in1}$ and $L_{in2}$ are charged by input DC source. And, the energy stored in inductor $L_{in2}$ is delivered to output port through $D_1$. This stage ends when $S_2$ is turned on with ZCS.

Because the playing role of both boost converter in proposed rectifier is only exchanged between stage 1 to state 8 and state 9 to state 16. The operation principle of state 9 to state 16 are the same state 1 to state 8. Thus, the state descriptions of state 9 to state 16 are neglected for simplifying the description.

After stage 16, the circuit operation is returned to the first stage. The voltage of the resonant capacitor $C_r$ is equaled to zero, and the resonant currents of the resonant inductors also equal zero. Thus, the assumption previously made is proven to be valid.

![Ideal relevant waveforms of proposed ZCS-PWM interleaved boost rectifier](image)

**Fig. 3 Ideal relevant waveforms of proposed ZCS-PWM interleaved boost rectifier.**

### III. REALIZATION AND EXPERIMENTAL RESULTS

To experimentally characterize the soft-switching properties of the ZCS-PWM interleaved boost rectifier, a breadboard was constructed to the specifications listed below:

- AC input voltage: 110 V
- DC output voltage: 400 VDC
- Output power: 1000W maximum
- Switching frequency: 40kHz

The experimental converter was constructed using the following components:

- Input inductors $L_1$ and $L_2$: 625uH
- Output capacitor $C_o$: 470uF
- Resonant inductors $L_{r1}$, $L_{r2}$, $L_{r3}$: 14μH
- Resonant capacitor $C_r$: 32nF
- Main power switches $S_1$, $S_2$: IRG4PC50UD
- Main power diodes $D_1$, $D_2$: S20LC20U
- Auxiliary power switch $S_3$: IRG4PC50UD
- Auxiliary power diodes $D_{a1}$, $D_{a2}$: HER308

The waveforms of the input voltage and current of the proposed rectifier are shown in Fig. 4(a), in which the waveforms of the input voltage and current are almost in phase and the measured power factor is over 0.99. The current waveforms $i_{in}$, $i_{in1}$, $i_{in2}$ are measured and shown in Fig. 4(b). The experimental result shown in Fig. 4(b) demonstrates that the input current ripple is certainly smaller than inductor current ripples. The commutation phenomenon in the main switches $S_1$ and $S_2$, main diodes $D_1$ and $D_2$ are measured in Fig. 5 and Fig. 6, respectively. The experimental results shown in Fig. 5 and Fig. 6 demonstrate that ZCS are achieved at constant frequency for these active switches ($S_1$, $S_2$). It should be noticed that the main diodes $D_1$ and $D_2$ were also softly commutated under ZCS. Therefore, the switching losses for the main switches and the main diodes in proposed ZCS-PWM interleaved boost rectifier are practically zero.

![Input voltage ($V_{in}$) and current input ($I_{in}$)](image)

**Fig. 4 (a) Input voltage ($V_{in}$) and input current ($I_{in}$). $V_{in}$: 100V/div; $I_{in}$: 10A/div, time: 4ms. (b) current ripple waveforms $i_{in1}$, $i_{in2}$: 10A/div, time: 10μs.**

### IV. CONCLUSION

A ZCS-PWM interleaved boost rectifier has been proposed in this paper. The circuit operation about the
The proposed rectifier has been analyzed. The power switches and diodes in proposed rectifier operate at ZCS turn on and off. The proposed rectifier uses the conventional PWM technique with constant operation frequency to regulate output voltage. Therefore, the proposed ZCS-PWM interleaved boost rectifier has advantages of the PWM and ZCS techniques. High power efficiency over 93% is acquired under the rated power of 1000W for proposed ZCS-PWM interleaved boost rectifier. Some experiment results prove the truth of the theoretical prediction.

![Fig. 5 Commutation in the main switches S1 and S2](a) VDS1: 250V/div; IDS1: 10A/div; time: 4μs/div

![Fig. 5 Commutation in the main switches S1 and S2](b) VDS2: 250V/div; IDS2: 10A/div; time: 4μs/div

![Fig. 6 Commutation in the main diodes D1 and D2](a) VD1, VD2: 500V/div; IDS1: 10A/div; time: 4μs/div

![Fig. 6 Commutation in the main diodes D1 and D2](b) VD1, VD2: 500V/div; IDS2: 10A/div; time: 4μs/div

REFERENCES


